MINI4412 Pin Definition

J0	Signal name	Function	Description	IO Type
1	GND	Ground		P
2	GND	Ground		P
3	GND	Ground		P
4	GND	Ground		P
5	VSYS	5V Power In	3.7-5.5V Wide power input	P
6	VSYS	5V Power In	3.7-5.5V Wide power input	P
7	VSYS	5V Power In	3.7-5.5V Wide power input	P
8	VSYS	5V Power In	3.7-5.5V Wide power input	P
9	V_SAVE	RTC battery in	2.4-6V Wide power input	P
10	GND	Ground		P
11	RST_KEY	Reset Key	Low Enable, Can NC it.	I
12	nRESET	System Reset	3.3V I/O	I/O
13	OM1	OM3: 1, Others: 0 Boot in EMMC&USB OM3/5: 1, Others: 0 Boot in EMMC&SD2		I
14	OM3			I
15	OM4			I
16	OM5			I
17	PWRHOLD	Power On Hold		O
18	GND	Ground		P
19	VDD_IO	3.3V Power In	3.3V +/- 5%	P
20	VDD_IO	3.3V Power In	3.3V +/- 5%	P
21	XpwmTOUT2	PWM Time Out2	GPD0_2 option	I/O
22	XpwmTOUT0	PWM Time Out0	LCD_FRM/GPD0_0 option	I/O
23	XpwmTOUT1	PWM Time Out1	LCD_PWM/GPD0_1 option	I/O
24	GND	Ground		P
25	XspiMOSI0	Spi Master out/Slave in	I2C_5_SCL/GPB3 option	I/O
26	XspiMISO0	Spi Master in/Slave out	I2C_5_SDA/GPB2 option	I/O
27	XspiCLK0	Spi CH0 Clock	I2C_4_SDA/GPB0 option	I/O
28	XspiCS0	Spi Chip Select	I2C_4_SCL/GPB1 option	I/O
29	XspiMISO1	Spi Master in/Slave out	GPB6 option	I/O
30	XspiMOSI1	Spi Master out/Slave in	GPB7 option	I/O
31	XspiCLK1	Spi CH1 Clock	IEM_SCLK/GPB4	I/O

32	XspiCS1	Spi Chip Select	IEM_SPWI/GPB5	I/O
33	XuRXD0	UART0_RXD/GPA0_0	Uart receives data input	I/O
34	XuTXD0	UART0_TXD/GPA0_1	Uart transmits data output	I/O
35	XuCTSn0	UART0_CTS/GPA0_2	Uart clear to send input signal	I/O
36	XuRTSn0	UART0_RTS/GPA0_3	Uart request to send output signal	I/O
37	XuRXD2	UART2_RXD/GPA1_0	Uart receives data input	I/O
38	XuTXD2	UART2_TXD/GPA1_1	Uart transmits data output	I/O
39	XuCTS2	UART2_CTS	I2C_3_SDA/GPA1_2 option	I/O
40	XuRTS2	UART2_RTS	I2C_3_SCL/GPA1_3 option	I/O
J1	**Signal name**	**Function**	**Description**	**IO Type**
1	SPDIF/XCLK	SPDIF or XCLK Output	SPDIF and XCLK Output option	O
2	GND	Ground		P
3	XhsicSTROBE0	USB_HSIC0_Srtobe		I/O
4	XhsicDATA0	USB_HSIC0_DATA		I/O
5	XotgDP	USB_OTG_DP	3.3V IO	I/O
6	XotgDM	USB_OTG_DM	3.3V IO	I/O
7	XVBUS	USB_OTG_VBUS	3.3V IO	I/O
8	USB_ID	USB_OTG_ID	3.3V IO	I/O
9	XotgDRV_VBUS	USB_OTG_DRVVBUS	3.3V IO	I/O
10	XEINT0	EINT0/GPX0_0	AUD_TCK option	I/O
11	XEINT1	EINT1/GPX0_1	AUD_TMS option	I/O
12	XEINT2	EINT2/GPX0_2	AUD_TDI option	I/O
13	XEINT3	EINT3/GPX0_3	AUD_TDO option	I/O
14	XEINT4	EINT4/GPX0_4	AUD_TRSTn option	I/O
15	XEINT5	EINT5/GPX0_5		I/O
16	XEINT6	EINT6/GPX0_6		I/O
17	XEINT7	EINT7/GPX0_7		I/O
18	XEINT9	EINT9/GPX1_1	KP_COL1 option	I/O
19	XEINT10	EINT10/GPX1_2	KP_COL2	I/O
20	XEINT11	EINT11/GPX1_3	KP_COL3	I/O
21	XEINT12	EINT12/GPX1_4	KP_COL4	I/O
22	XEINT13	EINT13/GPX1_5	KP_COL5	I/O
23	XEINT14	EINT14/GPX1_6	KP_COL6	I/O
24	XEINT15	EINT15/GPX1_7	KP_COL7	I/O
25	XEINT16	EINT16/GPX2_0	KP_ROW0 option	I/O
26	XEINT17	EINT17/GPX2_1	KP_ROW1	I
27	XEINT18	EINT18/GPX2_2	KP_ROW2	I/O
28	XEINT19	EINT19/GPX2_3	KP_ROW3	I/O
29	XEINT20	EINT20/GPX2_4	KP_ROW4	I/O

30	XEINT21	EINT21/GPX2_5	KP_ROW5	I/O
31	XEINT22	EINT22/GPX2_6	KP_ROW6	I/O
32	XEINT23	EINT23/GPX2_7	KP_ROW7	I/O
33	XEINT24	EINT24/GPX3_0	KP_ROW8	I/O
34	XEINT25	EINT25/GPX3_1	KP_ROW9	I/O
35	XEINT26	EINT26/GPX3_2	KP_ROW10	O
36	XEINT27	EINT27/GPX3_3	KP_ROW11	O
37	XEINT28	EINT28/GPX3_4	KP_ROW12	I/O
38	XEINT29	EINT29/GPX3_5	KP_ROW13	O
39	HDMI_CEC	EINT30/GPX3_6	Defined for HDMI CEC signal	I/O
40	HDMI_HPD	EINT31/GPX3_7	Defined for HDMI HPD signal	I/O
41	Xmmc2CLK	SD2_CLK/GPK2_0	3.3V IO	I/O
42	Xmmc2CMD	SD2_CMD/GPK2_1	3.3V IO	I/O
43	Xmmc2CDn	SD2_CDn/GPK2_2	3.3V IO	I/O
44	Xmmc2DATA0	SD2_DAT0/GPK2_3	3.3V IO	I/O
45	Xmmc2DATA1	SD2_DAT1/GPK2_4	3.3V IO	I/O
46	Xmmc2DATA2	SD2_DAT2/GPK2_5	3.3V IO	I/O
47	Xmmc2DATA3	SD2_DAT3/GPK2_6	3.3V IO	I/O
48	KP_COL0	KP_COL0/GPL2_0		I/O
49	SPEED	LAN_SPEED	Connoct to RJ45 Orange LED	O
50	LINK	LAN_LINK	Connoct to RJ45 Green LED	O
51	ETX+	TPO	Transmit Positive Output	O/I
52	ETX-	TNO	Transmit Negative Output	O/I
53	ERX+	RPI	Receive Positive Input	I/O
54	ERX-	RNI	Receive Negative Input	I/O
J2	**Signal name**	**Function**	**Description**	**IO Type**
1	Xmmc3CLK	SD3_CLK/GPK3_0		I/O
2	Xmmc3CMD	SD3_CMD/GPK3_1		I/O
3	Xmmc3CDn	SD3_CDn/GPK3_2		I/O
4	Xmmc3DATA0	SD3_DAT0/GPK3_3	SD2_DAT4 option	I/O
5	Xmmc3DATA1	SD3_DAT1/GPK3_4	SD2_DAT5 option	I/O
6	Xmmc3DATA2	SD3_DAT2/GPK3_5	SD2_DAT6 option	I/O
7	Xmmc3DATA3	SD3_DAT3/GPK3_6	SD2_DAT7 option	I/O
8	GND	Ground		P
9	KP_COL1	KP_COL1/GPL2_1		I/O
10	KP_COL2	KP_COL2/GPL2_2		I/O
11	KP_COL3	KP_COL3/GPL2_3		I/O
12	KP_COL4	KP_COL4/GPL2_4		I/O
13	KP_COL5	KP_COL5/GPL2_5		I/O

14	KP_COL6	KP_COL6/GPL2_6		I/O
15	KP_COL7	KP_COL7/GPL2_7		I/O
16	Xi2sSCLK0	I2S0_SCLK/GPZ0	I2S CH0 bus serial clock	I/O
17	Xi2sCDCLK0	I2S0_CDCLK/GPZ1	I2S CH0 Codec system clock	I/O
18	Xi2sLRCK0	I2S0_LRCLK/GPZ2	I2S CH0 bus channel select clock	I/O
19	Xi2sSDI0	I2S0_SDI/GPZ3	I2S CH0 bus serial data input	I/O
20	Xi2sSDO0	I2S0_SD0/GPZ4	I2S CH0 bus serial data0 output	I/O
21	Xi2sSDO1	I2S0_SD1/GPZ5	I2S CH0 bus serial data1 output	I/O
22	Xi2sSDO2	I2S0_SD2/GPZ6	I2S CH0 bus serial data2 output	I/O
23	XciBPCLK	CAMB_PCLK/GPM0_0	TS_CLK option	I/O
24	XciBVSYNC	CAMB_VSNC/GPM2_0		I/O
25	XciBHREF	CAMB_HREF/GPM2_1		I/O
26	XciBFIELD	CAMB_FIELD/GPM1_1		I/O
27	XciBMCLK	CAMB_MCLK/GPM2_2		I/O
28	XciBDATA0	CAMB_DATA0/GPM0_1	TS_SYNC option	I/O
29	XciBDATA1	CAMB_DATA1/GPM0_2	TS_VAL option	I/O
30	XciBDATA2	CAMB_DATA2/GPM0_3	TS_DATA option	I/O
31	XciBDATA3	CAMB_DATA3/GPM0_4	TS_ERROR option	I/O
32	XciBDATA4	CAMB_DATA4/GPM0_5		I/O
33	XciBDATA5	CAMB_DATA5/GPM0_6		I/O
34	XciBDATA6	CAMB_DATA6/GPM0_7		I/O
35	XciBDATA7	CAMB_DATA7/GPM1_0		I/O
36	XciAPCLK	CAMA_PCLK/GPJ0_0	Camera A clock in	I/O
37	XciAVSYNC	CAMA_VSYNC/GPJ0_1	Camera A VSYNC in	I/O
38	XciAHREF	CAMA_HREF/GPJ0_2	Camera A HSYNC in	I/O
39	XciADATA0	CAMA_DATA0/GPJ0_3	Camera A data 0 in	I/O
40	XciADATA1	CAMA_DATA1/GPJ0_4	Camera A data 1 in	IO
41	XciADATA2	CAMA_DATA2/GPJ0_5	Camera A data 2 in	I/O
42	XciADATA3	CAMA_DATA3/GPJ0_6	Camera A data 3 in	I/O
43	XciADATA4	CAMA_DATA4/GPJ0_7	Camera A data 4 in	I/O
44	XciADATA5	CAMA_DATA5/GPJ1_0	Camera A data 5 in	I/O
45	XciADATA6	CAMA_DATA6/GPJ1_1	Camera A data 6 in	I/O
46	XciADATA7	CAMA_DATA7/GPJ1_2	Camera A data 7 in	I/O
47	XciAMCLK	CAMA_MCLK/GPJ1_3	Master clock to dirver Camera	I/O
48	XciAFIELD	CAMA_FIELD/GPJ1_4	Reset or Power down Camera	I/O
49	Xmipi2LSDP1	MIPI2L_SDP1		I
50	Xmipi2LSDN1	MIPI2L_SDN1		I
51	Xmipi2LSDPCLK	MIPI2L_SDPCLK		I
52	Xmipi2LSDNCLK	MIPI2L_SDNCLK		I

53	Xmipi2LSDP0	MIPI2L_SDP0		I
54	Xmipi2LSDN0	MIPI2L_SDN0		I
J3	**Signal name**	**Function**	**Description**	**IO Type**
1	XadcAIN0	ADC_IN0		I
2	XadcAIN1	ADC_IN1		I
3	TXCP	HDMI_TXCP		O
4	TXCN	HDMI_TXCN		O
5	TX0P	HDMI_TX0P		O
6	TX0N	HDMI_TX0N		O
7	TX1P	HDMI_TX1P		O
8	TX1N	HDMI_TX1N		O
9	TX2P	HDMI_TX2P		O
10	TX2N	HDMI_TX2N		O
11	GND	Ground		P
12	XvHSYNC	LCD_HSYNC/GPF0_0		I/O
13	XvVSYNC	LCD_VSYNC/GPF0_1		I/O
14	XvVDEN	LCD_VDEN/GPF0_2		I/O
15	XvVCLK	LCD_VCLK/GPF0_3		I/O
16	XvVD0	LCD_VD0/GPF0_4		I/O
17	XvVD1	LCD_VD1/GPF0_5		I/O
18	XvVD2	LCD_VD2/GPF0_6		I/O
19	XvVD3	LCD_VD3/GPF0_7		I/O
20	XvVD4	LCD_VD4/GPF1_0		I/O
21	XvVD5	LCD_VD5/GPF1_1		I/O
22	XvVD6	LCD_VD6/GPF1_2		I/O
23	XvVD7	LCD_VD7/GPF1_3		I/O
24	XvVD8	LCD_VD8/GPF1_4		I/O
25	XvVD9	LCD_VD9/GPF1_5		I/O
26	XvVD10	LCD_VD10/GPF1_6		I/O
27	XvVD11	LCD_VD11/GPF1_7		I/O
28	XvVD12	LCD_VD12/GPF2_0		I/O
29	XvVD13	LCD_VD13/GPF2_1		I/O
30	XvVD14	LCD_VD14/GPF2_2		I/O
31	XvVD15	LCD_VD15/GPF2_3		I/O
32	XvVD16	LCD_VD16/GPF2_4		I/O
33	XvVD17	LCD_VD17/GPF2_5		I/O
34	XvVD18	LCD_VD18/GPF2_6		I/O
35	XvVD19	LCD_VD19/GPF2_7		I/O
36	XvVD20	LCD_VD20/GPF3_0		I/O

37	XvVD21	LCD_VD21/GPF3_1		I/O
38	XvVD22	LCD_VD22/GPF3_2		I/O
39	XvVD23	LCD_VD23/GPF3_3		I/O
40	AC97_BCLK	I2S1_SCLK/GPC0_0	PCM1_SCLK set for Buletooch	I/O
41	AC97_RST	I2S1_CDCLK/GPC0_1	PCM1_EXTCLK set for Buletooch	I/O
42	AC97_SYNC	I2S1_LRCLK/GPC0_2	PCM1_FSYNC set for Buletooch	I/O
43	AC97_SDI	I2S1_SDI/GPC0_3	PCM1_SIN set for Buletooch	I/O
44	AC97_SDO	I2S1_SDO/GPC0_4	PCM1_SOUT set for Buletooch	I/O
45	XuRXD1	RXD1/GPA0_4		I/O
46	XuTXD1	TXD1/GPA0_5		I/O
47	XuCTSn1	CTSn1/GPA0_6	I2C_2_SDA option	I/O
48	XuRTSn1	RTSn1/GPA0_7	I2C_2_SCL option	I/O
49	Xi2cSDA0	I2C_0_SDA/GPD1_0		I/O
50	Xi2cSCL0	I2C_0_SCL/GPD1_1		I/O
51	Xi2cSDA1	I2C_1_SDA/GPD1_2		I/O
52	Xi2cSCL1	I2C_1_SCL/GPD1_3		I/O
53	XuRXD3	RXD3/GPA1_4	UART_AUDIO_RXD option	I/O
54	XuTXD3	TXD3/GPA1_5	UART_AUDIO_TXD option	I/O